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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,875	03/31/2004	Yu-Pin Chou	3722-0186PUS1	4577

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,875	CHOU ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *31 March 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 is indefinite because of the recited limitation "the delay from the first input signal to the reset of the phase error detecting unit is substantially the same as the delay from the first input signal to the first flag signal" is unclear because it cannot be determined what the delay means. Insofar as understood, the first input signal (Fr in instant Fig. 5) is the clock signal to the flip-flop 411; the reset of the phase error detecting unit is the input terminal RB of 402; and first flag signal FLAG_1 is the output terminal of 401. Since the clock signal is not transferred to those terminals so it is unclear as to what the claimed limitation of "the delay" means.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6, 7, and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsinker (US 6,323,692).

With regard to claims 1 and 2, Tsinker discloses in Figs. 1 and 10 a phase frequency detector (28) comprising a phase error detecting unit (202, 204, 210) for outputting at least a phase error signal (30, 34) according to a phase error between a first input signal (REF. CLOCK) and a second input signal (FILTER CLOCK); and a reset unit (206-210) coupled to the phase error detecting unit for receiving the first input signal and the second input signal, and for outputting a reset signal (UPDN_RST) according to the first input signal and the second input signal, in order to reset the phase error detecting unit.

With regard to claim 3, the phase error detecting unit comprises a first flip-flop (202) for outputting a first flag signal (UP) according to the first input signal (REF. CLOCK); and a second flip-flop (204) for outputting a second flag signal (DN) according to the second input signal (FILTER CLOCK).

With regard to claim 4, the phase error detecting unit further comprises a sampling circuit (210) for outputting the phase error signal according to the first flag signal and the second flag signal.

With regard to claim 6, the reset signal comprises a first reset signal (RESET_UP) for resetting the first flip-flop (202); and a second reset signal (RESET_DN) for resetting the second flip-flop (204).

With regard to claim 7, the reset unit comprises a third flip-flop (208) for outputting the second reset signal according to the first input signal; and a fourth flip-flop (206) for outputting the first reset signal according to the second input signal.

With regard to claim 9, the reference also meets the recited limitations in the claim.

With regard to claim 10, Tsinker discloses in Figs. 1 and 4 a phase locked loop (10) comprising a phase error detector (28) for receiving a first input signal (REF. CLOCK) and a second input signal (FILTER CLOCK) and outputting a phase error signal (30, 34); and a clock signal generator (32, 36, 22, 224) for outputting the second input signal according to the phase error signal; wherein the phase error detector comprises a phase error detecting unit (150, 152) for outputting the phase error signal according to a phase error between the first input signal and the second input signal; and a reset unit (154 - 158) coupled to the phase error detecting unit for receiving the first input signal and the second input signal, and for outputting a reset signal (RST) according to the first input signal and the second input signal, in order to reset the phase error detecting unit.

With regard to claim 11, the reference also meets the recited limitations in the claim.

5. Claims 1, 2, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (US 6,326,826).

With regard to claims 1 and 2, Lee et al. discloses in Figs. 1-4 a phase frequency detector comprising a phase error detecting unit (41, 42) for outputting at least a phase error signal (PUP) according to a phase error between a first input signal (REF_CK) and a second input signal (CK[7]); and a reset unit coupled to the phase error detecting unit for receiving the first input signal and the second input signal, and for outputting a reset signal according to the first input signal and the second input signal, in order to reset the phase error detecting unit.

With regard to claim 8, the phase error detecting unit further comprises a buffer circuit (the inverters in series) for buffering the first input signal and the second input signal.

With regard to claim 9, the reference also meets the recited limitations in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsinker in view of the admitted prior art, Figs. 1A & 1B in the present application.

The above-discussed circuit of Tsinker meets all of the claimed limitations except that the phase error detector is implemented in the phase locked loop having a different type of clock signal generator from the clock signal generator recited in these claims. The admitted prior art teaches a phase locked loop having a clock signal generator as recited in these claims. Therefore, it would have been obvious to one of ordinary skill in the art that **the** phase error detector of Tsinker can be implemented in the phase locked loop accordance with the principle teaching of the prior art, Figs. 1A & 1B in the present application, in order to meet the specific condition of the particular application.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. McDonagh (US 6,239,634) is cited as of interest because it discloses an apparatus and method for ensuring the correct start-up and locking of a delay locked loop.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
May 25, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800